# Solutions - Homework 1

(Due date: January 17th @ 7:30 pm)
Presentation and clarity are very important! Show your procedure!

## PROBLEM 1 (50 PTS)

- Leading Zero Detector: This iterative circuit processes a 15-bit input (MSB first) and generates the number of leading 0's. before the first 1. Example:
  - ✓ If the sequence is: 0000 0000 0011 010 → R = 10
  - ✓ If the sequence is: 0001 0000 0011 010 → R = 3
  - ✓ If the sequence is: 0000 0000 1000 001 → R = 8

- The figure depicts the (in ASM form) and a datapath circuit. Note: Counters. If E=sclr=1, → Q=0.
  Input data: x (entered sequentially, MSB first). Output data R.

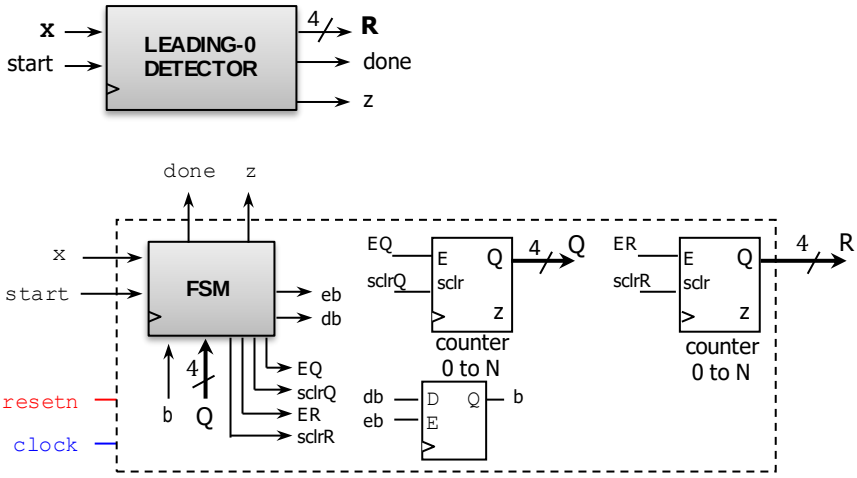
  - ✓ Complete the timing diagram of the digital circuit (next page). Note that 3 sequences are evaluated.

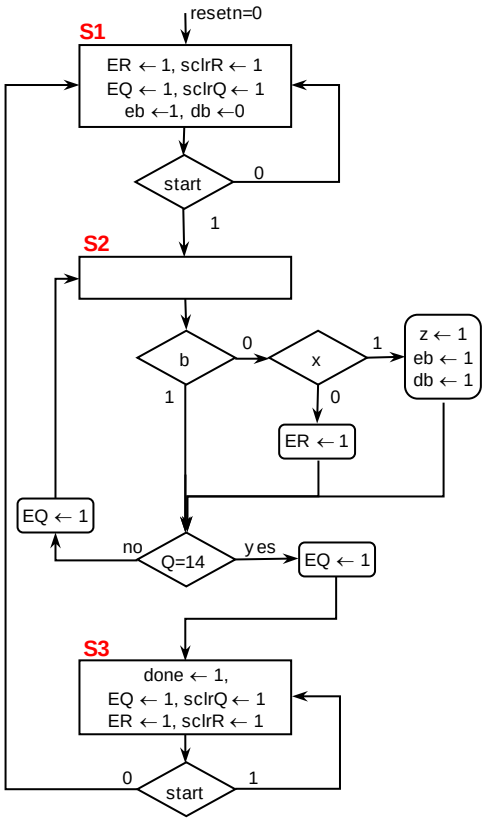
  - ✓ Write a structural VHDL code. You MUST create a file for i) modulo-(N+1) counter, ii) flip-flop, iii) Finite State Machine, and v) Top file (where you will interconnect all the components).

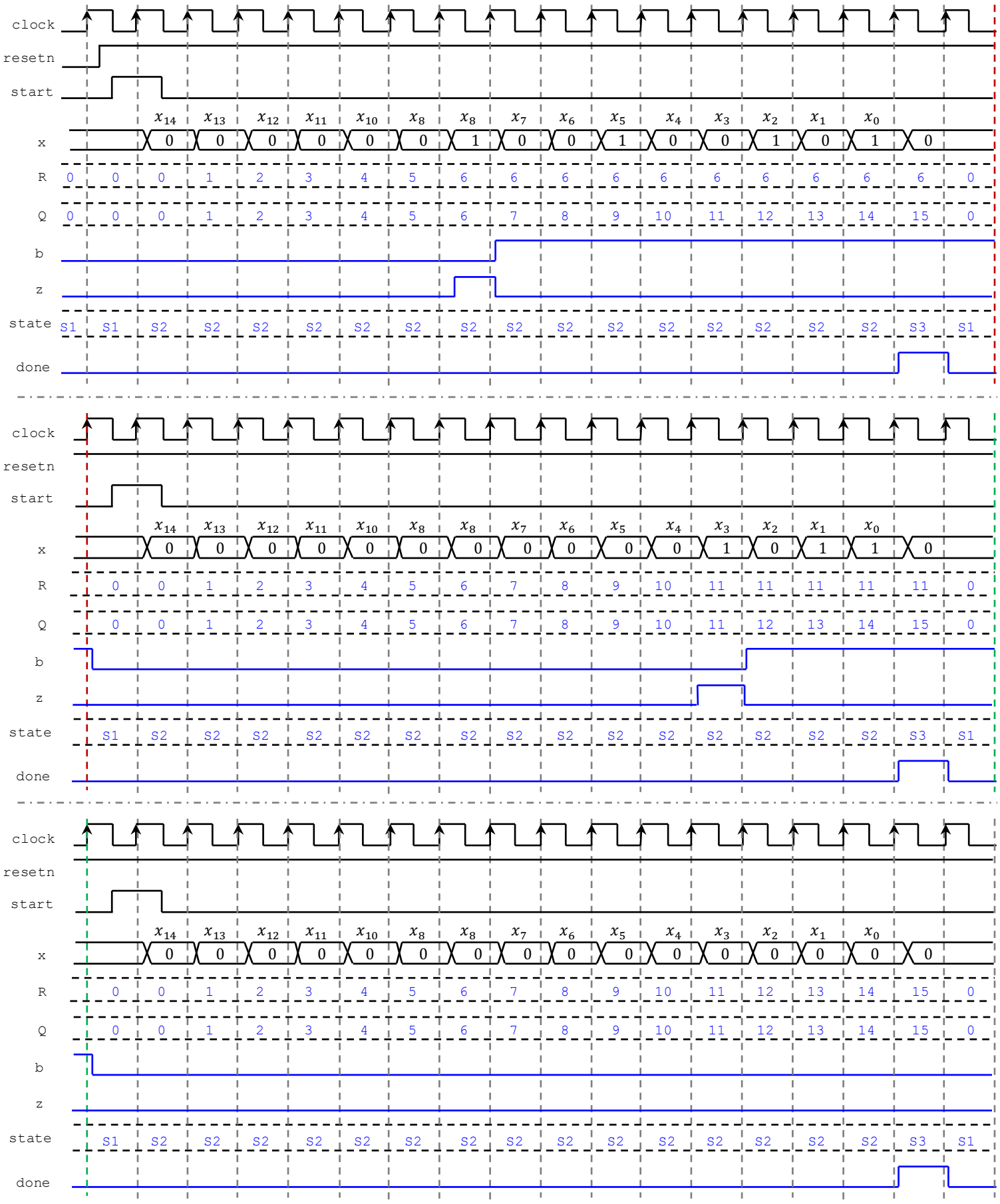
  - ✓ Write a testbench according to the timing diagram shown (next page). Simulate the circuit (Behavioral simulation). Verify that the simulation is correct by comparing it with the timing diagram you completed manually.

  - ✓ Upload the following files to Moodle (an assignment will be created):
    - VHDL code files
    - VHDL testbench

    See attached .zip file: `SolutionsHW1p1.zip`



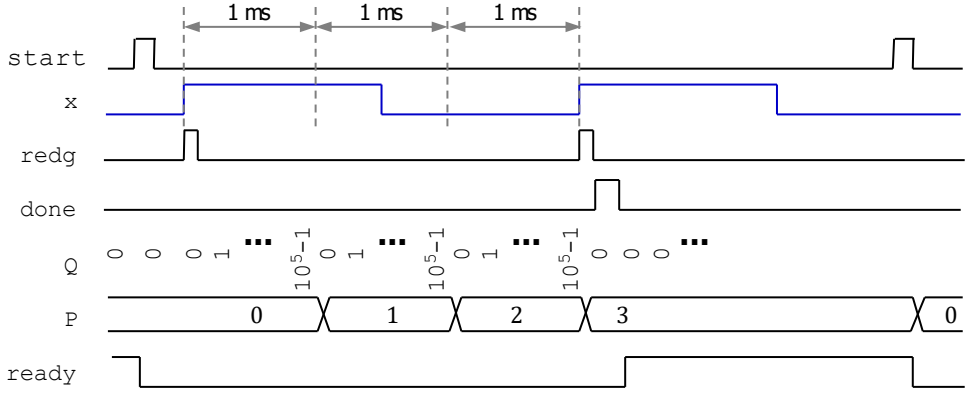




clock
resetn
start
x
R
Q
b
z
state
done
$x_{14}$ $x_{13}$ $x_{12}$ $x_{11}$ $x_{10}$ $x_8$ $x_8$ $x_7$ $x_6$ $x_5$ $x_4$ $x_3$ $x_2$ $x_1$ $x_0$
0 0 0 0 0 0 1 0 0 1 0 0 1 0 1 0
0 0 0 1 2 3 4 5 6 6 6 6 6 6 6 6 6 6 0
0 0 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0
S1 S1 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S3 S1
clock
resetn
start
x
R
Q
b
z
state
done
$x_{14}$ $x_{13}$ $x_{12}$ $x_{11}$ $x_{10}$ $x_8$ $x_8$ $x_7$ $x_6$ $x_5$ $x_4$ $x_3$ $x_2$ $x_1$ $x_0$
0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0
0 0 1 2 3 4 5 6 7 8 9 10 11 11 11 11 11 0
0 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0
S1 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S3 S1
clock
resetn
start
x
R
Q
b
z
state
done
$x_{14}$ $x_{13}$ $x_{12}$ $x_{11}$ $x_{10}$ $x_8$ $x_8$ $x_7$ $x_6$ $x_5$ $x_4$ $x_3$ $x_2$ $x_1$ $x_0$
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0
0 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0
S1 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S2 S3 S1

# PROBLEM 2 (30 PTS)

- **Period Counter**: It measures the period of a periodic input waveform with a precision of 1 ms (from 1 ms to 1000 ms).
  - ✓ Inputs: x (input waveform), s (start signal).
  - ✓ Outputs: P (period in ms), done, and ready (ready to take a measurement)
  - ✓ Clock frequency: 100 Mhz.


- Operation: The circuit takes a measurement when the s signal (usually a clock pulse) is asserted. This amounts to count the number of cycles between two rising edges of the input waveform.
- However, to directly count the number of milliseconds, we can use a counter Q that counts up to 1 ms. Every time Q reaches 1 ms, we increase the count on another counter P, which will keep the number of milliseconds elapsed.
- The counter Q starts counting after the first rising edge is detected. When the second rising edge is detected, we assert done for a clock cycle. We are then ready to measure again should the signal s is asserted. The figure below shows an example for an input waveform whose period is 3 ms.

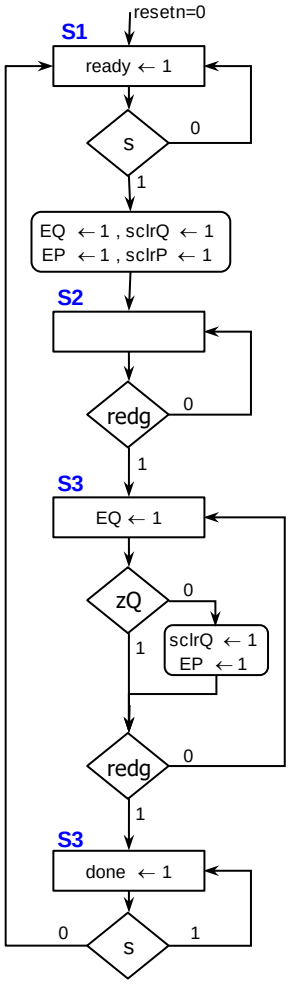



✓ Sketch the circuit: FSM + Datapath components. Specify all the I/Os of the FSM, as well as the signals connecting the FSM and the Datapath components.

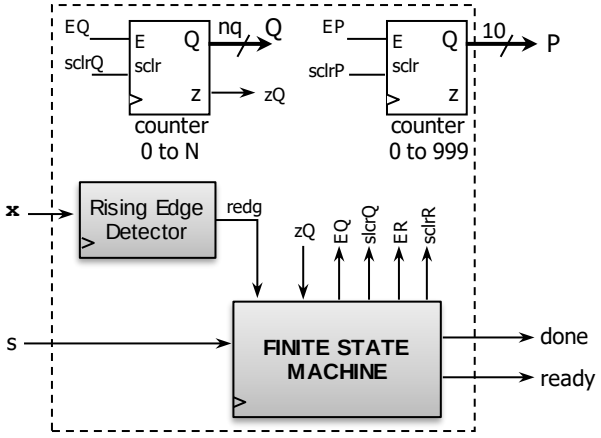
Suggestion: The Datapath only needs two counters (Q and R) and a rising edge detector.

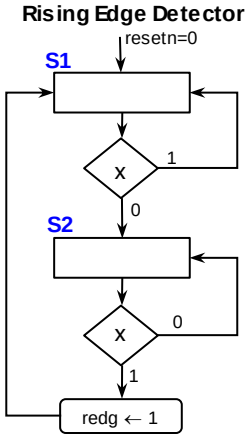
- Rising edge detector: It issues a one-cycle (10 ns) pulse on redg when it detects a rising edge on x.
- Counter Q: 1 ms counter. For a clock period of 10 ns, it counts from 0 to $10^5$-1.
- Counter P: It stores the period of x in ms. This counter counts from 0 to 999.

You can use the standard counter with *enable* and *sclr* inputs.
If using a rising edge detector block, sketch its design (e.g.: State Machine)




✓ Provide the State Diagram (in ASM form) of the FSM.

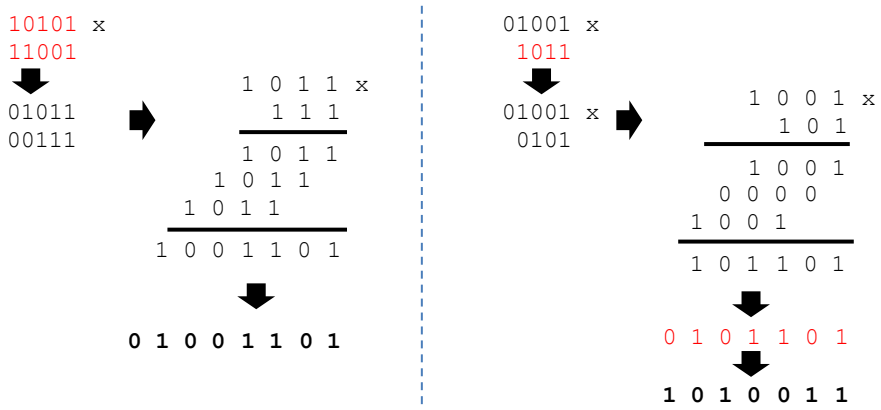


# PROBLEM 3 (20 PTS)

- Calculate the result of the following operations, where the operands are signed integers. For the division, calculate both the quotient and the residue. **No procedure ≡ zero points.**

| | | | | |
|---|---|---|---|---|
| 10101 × 11001 | 01001 × 1011 | 101001 ÷ 10101 | 0111101 ÷ 10110 | 10011 ÷ 0111 |




✓ $\frac{101001}{10101} = \frac{-23}{-11}$

To unsigned: $\frac{010111}{01011}$

```
      00010
1011 ) 10111
       1011
         01
```

Unsigned Integer Division: $Q' = 10, R' = 1$
$\rightarrow Q = Q' = 010, \rightarrow R = -R' = 2C(01) = 1$

Verification: $-23 = (-11 \times 2) - 1$

✓ $\frac{0111101}{10110} = \frac{61}{-10}$

To unsigned: $\frac{0111101}{01010}$

```
      000110
1010 ) 111101
       1010
        1010
        1010
          01
```

Unsigned Integer Division: $Q' = 110, R' = 1$
$\rightarrow Q = -Q' = 2C(0110) = 1010, \rightarrow R = R' = 01$

Verification: $61 = (-10 \times -6) + 1$

✓ $\frac{10011}{0111} = \frac{-13}{7}$

To unsigned: $\frac{01101}{0111}$

```
      0001
111 ) 1101
      111
      110
```

Unsigned Integer Division: $Q' = 1, R' = 110$
$\rightarrow Q = -Q' = 2C(01) = 1, \rightarrow R = -R' = 2C(0110) = 1010$

Verification: $-13 = (7 \times -1) - 6$